AMENDMENT TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) A method for forming a stacked package of at least an upper semiconductor package unit and a lower semiconductor package unit, the method comprising:

(a) flattening leads of said upper semiconductor package unit;

(b) shortening at least one selected lead of said upper semiconductor package unit such that the shortened said lead does not contact a lead of said lower semiconductor package unit when said upper semiconductor package unit is stacked atop said lower semiconductor package unit in a same orientation;

(c) stacking said upper semiconductor package unit on said lower semiconductor package unit in said same orientation;

(d) forming a direct electrical connection between two leads of said upper semiconductor package unit; ~~The method of claim 1, wherein step (d) includes forming said direct electrical connection~~ by soldering said two leads; and.

(e) forming direct electrical connections between leads of said upper semiconductor package unit and corresponding leads of said lower semiconductor package unit.

3. (Cancelled)

4. (Currently Amended) The method of claim 2~~1~~, wherein said upper and lower semiconductor package units have identical lead layouts.

5. (Cancelled)

6. (Currently Amended) A method for forming a stacked package of at least an upper semiconductor package unit and a lower semiconductor package unit wherein said upper semiconductor package unit has a chip-select (CS) lead and a not-connected (NC) lead, the method comprising:

(a) flattening leads of said upper semiconductor package unit;

(b) shortening at least one selected lead of said upper semiconductor package unit such that the shortened said lead does not contact a lead of said lower semiconductor package unit when said upper semiconductor package unit is stacked atop said lower semiconductor package unit in a same orientation;

(c) stacking said upper semiconductor package unit on said lower semiconductor package unit in said same orientation;

(d) forming a direct electrical connection between said CS lead and said NC lead;~~The method of claim 5, wherein step (d) includes forming said direct electrical connection~~ by soldering said CS lead and said NC lead; and

(e) forming direct electrical connections between leads of said upper semiconductor package unit and corresponding leads of said lower semiconductor package unit..

7. (Currently Amended) A method for forming a stacked package of at least an upper semiconductor package unit and a lower semiconductor package unit,~~The method of claim 1,~~ wherein said upper semiconductor package unit has a clock-enable (CKE) lead and a not-connected (NC) lead, the method comprising:

(a) flattening leads of said upper semiconductor package unit;

(b) shortening at least one selected lead of said upper semiconductor package unit such that the shortened said lead does not contact a lead of said lower semiconductor package unit when said upper semiconductor package unit is stacked atop said lower semiconductor package unit in a same orientation;

(c) stacking said upper semiconductor package unit on said lower semiconductor package unit in said same orientation;

(d) ~~and wherein step (d) further includes~~ forming a direct electrical connection between said CKE lead and said NC lead; and

(e) forming direct electrical connections between leads of said upper semiconductor package unit and corresponding leads of said lower semiconductor package unit.

8. (Original) The method of claim 7, wherein step (d) includes forming said direct electrical connection by soldering said CKE lead and said NC lead.

9. (Cancelled)

10. (Currently Amended) A method for forming a stacked package of at least an upper semiconductor package unit and a lower semiconductor package unit, ~~The method of claim 1,~~ wherein said upper semiconductor package unit has a clock-enable (CKE) lead, the method comprising:

(a) flattening leads of said upper semiconductor package unit;

(b) ~~and step (b) further includes~~ shortening a length of said CKE lead such that the shortened said CKE lead does not contact a lead of said lower semiconductor package unit when said upper semiconductor package unit is stacked atop said lower semiconductor package unit in a same orientation;

(c) stacking said upper semiconductor package unit on said lower semiconductor package unit in said same orientation;

(d) forming a direct electrical connection between two leads of said upper semiconductor package unit; and

(e) forming direct electrical connections between leads of said upper semiconductor package unit and corresponding leads of said lower semiconductor package unit.

11. (Cancelled)

12. (Currently Amended) A method for forming a stacked package of at least an upper semiconductor package unit and a lower semiconductor package unit, ~~The method of claim 1~~, wherein said upper semiconductor package unit has a clock-enable (CKE) lead~~-~~, the method comprising:

(a) flattening leads of said upper semiconductor package unit;

(b) shortening at least one selected lead of said upper semiconductor package unit such that the shortened said lead does not contact a lead of said lower semiconductor package unit when said upper semiconductor package unit is stacked atop said lower semiconductor package unit in a same orientation;

(c) stacking said upper semiconductor package unit on said lower semiconductor package unit in said same orientation;

(d) forming a direct electrical connection between two leads of said upper semiconductor package unit; and

(e) forming direct electrical connections between leads of said upper semiconductor package unit and corresponding leads of said lower semiconductor package unit, ~~and step (e)~~ excludinges selecting said CKE lead.

Claims 13-20. (Cancelled)

21. (New) A method for forming a stacked package of at least an upper semiconductor package unit and a lower semiconductor package unit, the method comprising:

(a) flattening leads of said upper semiconductor package unit;

(b) shortening at least one selected lead of said upper semiconductor package unit such that the shortened said lead does not contact a lead of said lower semiconductor package unit when said upper semiconductor package unit is stacked atop said lower semiconductor package unit in a same orientation;

(c) stacking said upper semiconductor package unit on said lower semiconductor package unit in said same orientation;

(d) forming a direct electrical solder connection between two adjacent leads of said upper semiconductor package unit; and

(e) soldering a direct electrical connections between adjacent leads of said upper semiconductor package unit and corresponding leads of said lower semiconductor package unit.

REMARKS

This Amendment and Response is submitted in response to the Office Action mailed 25 July 2003. Withdrawal of the rejection and reconsideration with an eye toward allowance is respectfully requested.

Claim Status

Claims 2, 4, 6-8, 10, 12, and 21 are pending after entry of the present amendment. Claims 1, 3-5, 9, and 11 stand rejected, and the Examiner has objected to claims 2, 6-8, 10 and 12. Claims 2, 4, 6, 7, 10 and 12 are amended herein, claims 1, 3, 5, 9, and 11 are cancelled herein, and claim 21 added. Support for the above claim amendments can be found in the specification, drawings, and claims as originally filed.

Claim Objections

The Examiner objected to claims 1 and 9 because of informalities. Claims 1 and 9 have been cancelled, obviating the objections.

Claim Rejections – 35 U.S.C. §102

Claims 1, 3-5, 9, and 11 were rejected under 35 U.S.C. §102(e) as being anticipated by Kang (U.S. Patent Number 6,242,285).

Without admitting the propriety of the rejection, Claims 1, 3, 5, 9 and 11 have been cancelled, without prejudice or disclaimer towards presenting them in a related application. Claim 4 has been amended to depend from and include all limitations of Applicants' claim 2, which has been amended to include allowable subject matter, as indicated by the Examiner. Accordingly, Applicants submit that the 35 U.S.C. §102 rejection of claims 1, 3-5, 9, and 11 has been obviated, and should be withdrawn. Applicants submit claim 4 is in condition for allowance.

Allowable Subject Matter

Applicants note with appreciation the Examiner's indication of allowable subject matter in claims 2, 6-8, 10 and 12. Applicants have amended claims 2, 6-7, 10 and 12 to put the claims in independent form. Claim 8 depends from amended claim 7. Accordingly, Applicants trust that claims 2, 6-8, 10 and 12 are now in condition for allowance. Further, as stated above, Applicants have amended claim 4 to depend from claim 2, and submit that claim 4 is also in condition for allowance.

New Claim

Applicants have added new claim 21, and submit that new claim 21 is patentable over the cited art for at least the reasons given by the Examiner in the indication of allowable subject matter. Accordingly, Applicants submit that new claim 21 is in condition for allowance.

CONCLUSION

Applicants submit the claims are in condition for allowance, and notification of such is respectfully requested. If after review, the Examiner feels there are further unresolved issues, the Examiner is invited to call the undersigned at (415) 781-1989.

Respectfully submitted,
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